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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,523	KWAG, JIN-OH	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 7-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 7-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 28, 2005 has been entered. An action on the RCE follows:

2. This office action is made in response to applicant's amendment/argument filed on October 26, 2005. Claims 4, 6, 25, 26 are cancelled, claims 1-3, 5 and 7-24 are amended. Thus, claims 1-3, 5 and 7-24 are currently pending in the application.

3. The rejection of claims 15-24 under 35 U.S.C. 112, second paragraph, is withdrawn.

4. Claim 14 is objected to under 37 CFR 1.75(a) because although these claims meet the requirement 112/2d, i.e., the metes and bounds are determinable, however, claim 14 should be read "the reset interval is starts about 0.5ms to about 5ms" (based on the specification, applicant pointed out at page 4, line 18). It is in the best interest of the patent community that applicant, in his/her normal review and/or rewriting of the claims, to take into consideration these editorial situations and make changes as necessary.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5 and 7-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al (US 6,046,790) hereinafter Hara in view of McKnight (US 5,920298).

6. As to claims 1 and 5, Hara teaches a liquid crystal display (LCD) device associated with a method, the LCD device comprising:

a plurality of gate lines [a plurality of gate lines 2, see Fig. 14, col. 34, lines 35-39];

a plurality of data lines intersecting the gate lines [a plurality of signal lines 4, see Fig. 14, col. 34, lines 35-39];

a data driver generating data voltage for the data lines [a signal line driver 22, fig. 14, col. 34, lines 59-62];

a gate driver generating stepped-wave pattern gate signals for the gate lines [a gate line driver 21, fig. 14, col. 34, lines 59-62], each stepped-wave pattern gate signal [fig. 3] including a reset interval [a reset selection time Tr, Fig. 16A, col. 33, line 42], a gate-on interval following the reset interval [a gate selection time T_{gon}, see Fig. 16A, col. 33, lines 41-44], and an overshoot-interval following the gate-on interval and having the

same polarity with a data voltage applied to the pixel [a frame period T_{frame}, see Fig. 33, col. 33, lines 50-57].

Accordingly, Takenaka teaches all of the claimed limitation, except for a reset interval for converting a grayscale level of a pixel corresponding to a subsequent gate line to an extreme grayscale level.

However, McKnight teaches one reset pulse 600 is presented to pixels 601-604, they undergo a rapid drive-to-dark 612 at time t1. The intensities 1-4 then increase to their respective grey levels 611. As depicted, pixel 604 is driven to the brightest grey level (see Fig. 6A, col. 9, lines 59-65).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the a reset pulse 600 for converting a grayscale level of a pixel 604 corresponding to a subsequent gate line to the brightest grayscale level as taught by McKnight in the driving waveform of Hara in order to achieve the benefit to intend to drive the LCD device, because this would improve the high image contrast and brightness (McKnight, col. 3, lines 1-3), and this improvement aids rapid switching between grey levels (McKnight, col. 3, lines 49-50).

7. As to claims 2 and 3, McKnight teaches wherein the extreme grayscale level is a black grayscale level in a normally white mode [they undergo a rapid drive-to-dark 612 at time t1. The intensities 1-4 then increase to their respective grey levels 611. As depicted, pixel 604 is driven to the brightest grey level, see Fig. 6A, col. 9, lines 59-65].

8. As to claim 7, Hara teaches wherein the gate signal in the reset interval has the same polarity with the gate signal in the overshoot interval [see Figs. 16A and 16C].

9. As to claim 8, Hara teaches wherein the gate signal in the reset interval has a different polarity with the gate signal in the overshoot interval [see figs. 13A and 13B].

10. As to claim 9, Hara teaches wherein a voltage level of the gate signal in the overshoot interval is +3V to +10V relative to a gate-off voltage [the maximum voltage D applied between the pixel electrode and the counter electrode is 5V, col. 33, lines 53-55].

11. As to claim 10, Hara teaches wherein the overshoot interval starts when the gate-on interval ends, and converts to a gate-off voltage when the gate-on interval doubles [the gate pulse voltage, V_{gon} is set at +30 V, V_{goff} is set at –10V, see Fig. 13A, col. 33, lines 50-51].

12. As to claims 11 and 12, McKnight teaches wherein the extreme grayscale level is a black grayscale level in a normally white mode [they undergo a rapid drive-to-dark 612 at time t1. The intensities 1-4 then increase to their respective grey levels 611. As depicted, pixel 604 is driven to the brightest grey level, see Fig. 6A, col. 9, lines 59-65].

13. As to claim 13, Hara teaches wherein a voltage level of the gate signal in the reset interval is +3V to +10V relative to a gate-off voltage [during the period of reset period Tr, the V_{gon} is et at +30V and V_{goff} is set at –10V, see Fig. 13A, col. 33, lines 45-51. It would have been obvious to provide a gate voltage level is in the range of +3V to +10V].

14. As to claim 14, Hara teaches wherein the reset interval start about 0.5ms to about 5ms after the gate-on interval starts [the reset selection time Tr is set at 5 times the T_{gon}, that is , 170μs, see col. 35, lines 19-20].

15. As to claim 15, Hara teaches a liquid crystal display, comprising:

a gate line generating a gate signal [a gate line driver 21, Fig. 14];

a data driver generating a first data voltage and a second data voltage [a signal line 4, Fig. 14];

a first gate line transmitting the gate signal [a first gate line 2-1, Fig. 14];

a second gate line neighboring the fist gate line and transmitting the gate signal [a second gate line 2-2, Fig. 14];

a data line intersecting the first and second gate lines and transmitting the first data signal and the second data signal [a data signal lines 4-1 and 4-2, Fig. 14];

A first switching element connected to the first gate line and the data line and selectively transmitting the first data voltage to a first pixel [a first switching element 5-1, Fig. 14, col. 34, lines 35-55];

a second switching element connected to the second date line and the data line and selectively transmitting the second data voltage to a second pixel [a first switching element 5-2, Fig. 14, col. 34, lines 35-55];

a first liquid crystal capacitance formed at the first pixel [a first liquid crystal capacitance C_{LC} 23-1, Fig. 3];

a second liquid crystal capacitance formed at the first pixel [a first liquid crystal capacitance C_{LC} 23-2, Fig. 3];

a storage capacitance formed between the second liquid crystal capacitance and the first gate line [a C_s 12, Fig. 3];

wherein the gate signal applied to the first gate line has a first interval [a reset selection time Tr, Fig. 16A], a second interval [a gate selection time Tgon, Fig. 16A] following the first interval and having a second voltage, a third interval [a frame period Tframe, Fig. 16A] following the second interval and having a third voltage and a fourth interval [the rest interval, Fig. 16B, col. 35, line 14] following the third interval and having a fourth voltage [see col. 35, lines 10-21];

Accordingly, Takenaka teaches all of the claimed limitation, except wherein the gate signal applied to the first gate line has a first interval having a first voltage converting a grayscale level of the second pixel to an extreme grayscale level,

However, McKnight teaches the first interval (one reset pulse 600) is presented to pixels 601-604, they undergo a rapid drive-to-dark 612 at time t1. The intensities 1-4 then increase to their respective grey levels 611. As depicted, pixel 604 is driven to an extreme grayscale level (the brightest grey level) (see Fig. 6A, col. 9, lines 59-65).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the a reset pulse 600 for converting a grayscale level of a pixel 604 corresponding to a subsequent gate line to the brightest grayscale level as taught by McKnight in the driving waveform of Hara in order to achieve the benefit to intend to drive the LCD device, because this would improve the high image contrast and brightness (McKnight, col. 3, lines 1-3), and this improvement aids rapid switching between grey levels (McKnight, col. 3, lines 49-50).

16. As to claim 16, Hara teaches wherein the first switching element is turned on by the second voltage and turned off by the fourth voltage [the gate pulse voltage, V_{gon} is set at +30 V, V_{goff} is set at –10V, see Fig. 13A, col. 33, lines 50-51].

17. As to claim 17, Hara further teaches the common line providing a common voltage [counter electrode 16 connected to ground, Fig. 3, col. 24, line 60-67] for the first liquid crystal capacitance and the second liquid crystal capacitance [the pixel matrix comprises a first liquid crystal capacitance C_{LC} and a second liquid crystal capacitance C_{LC}, Fig. 10, col. 30, lines 1-34], wherein the third voltage of the gate signal applied to the first gate line is greater than the fourth voltage when the first data voltage is higher than the common voltage, and the third voltage of the gate signal applied to the first gate line is lower than the fourth voltage when the first data voltage is less than the common voltage [Figs. 11 (a), (b), (c), and (d), col. 30, line 35 through col. 31, line 56].

18. As to claim 18, Hara further teaches wherein both the first and third voltage are higher or lower than the fourth voltage [Figs. 11 (a), (b), (c), and (d), col. 30, line 35 through col. 31, line 56].

19. As to claim 19, Hara further teaches wherein the LCD operates in a normally white mode [the LCD operates at minimum brightness, col. 35, line 27].

20. As to claim 20, Hara further teaches wherein one of the first and the third voltage is greater than the fourth voltage and the other is less than the fourth voltage [Figs. 11 (a), (b), (c), and (d), col. 30, line 35 through col. 31, line 56].

21. As to claim 21, Hara further teaches wherein the LCD operates in a normally black mode [the LCD operates at maximum brightness, col. 35, line 27].

22. As to claim 22, Hara further teaches wherein both the first and third voltage are higher or lower than the fourth voltage [Figs. 11 (a), (b), (c), and (d), col. 30, line 35 through col. 31, line 56].

23. As to claim 23, Hara further teaches wherein a level of the third voltage is between levels the first voltage and the fourth voltage [Figs. 11 (a), (b), (c), and (d), col. 30, line 35 through col. 31, line 56].

24. As to claim 24, Hara further teaches wherein one of the first and the third voltage is greater than the fourth voltage and the other is less than the fourth voltage [Figs. 11 (a), (b), (c), and (d), col. 30, line 35 through col. 31, line 56].

Response to Arguments

25. Applicant's arguments with respect to claims 1-3, 5 and 7-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, a supervisor Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the

Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197

(toll-free).

Kevin M. Nguyen
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Art Unit 2674

KMN
February 20, 2006